REMARKS

Claims 1–20 are pending in the present application. Claim 20 was withdrawn from consideration as directed to a non-elected species.

Claims 2–19 were amended.

Claim 2 was amended to consolidate the limitations of claims 2–3; claim 4 was amended to consolidate the limitations of claims 4 and 9; claim 5 was amended to consolidate the limitations of claims 5–8; and claims 15 and 16 were amended to consolidate the limitations of claims 14–15 and 16–17, respectively. The scope of the pending claims was not changed by these amendments.

Claim 3, 6–9, 14 and 17 were amended to introduce a features not previously presented in the claims.

Claims 10 and 18 were amended for clarity and for consistency with terminology in other claims. The scope of these claims was not narrowed by these amendments.

Claim 11 was amended for clarity of terminology and consistency with ordinary meanings ascribed to certain terms in the relevant art. The scope of the claim was not narrowed by this amendment.

Claim 12 was amended to clarify the meaning of the claim term "profile", without altering the scope of the claim; claim 19 was amended to eliminate the indefinite claim term "profile" and to broaden the claim.

Claim 13 was amended for clarity of terminology and consistency with ordinary meanings ascribed to certain terms in the relevant art, and also to broaden the claim. The scope of the claim was not narrowed by this amendment.

Reconsideration of the claims is respectfully requested.

35 U.S.C. § 112, First Paragraph (Written Description)

Claims 12 and 19 were rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter not which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time of the application was filed, had possession of the claimed invention. This rejection is respectfully traversed.

Claims 12 and 19 have been amended to eliminate the indefinite term "profile."

Therefore, the rejection of claims 12 and 19 under 35 U.S.C. § 112, first paragraph has been overcome.

35 U.S.C. § 102 (Anticipation)

Claims 1, 4, 10–11, 13, 16 and 18 were rejected under 35 U.S.C. § 102(a) as being anticipated by U.S. Patent No. 5,677,567 to *Ma et al.* This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed

invention is found in a single prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

Independent claims 1 and 13 each recite that the second (integrated circuit) chip is mounted on the active face of the first (integrated circuit) chip. Such a feature is not shown or suggested by the cited reference. The cited portion of *Ma et al* discloses integrated circuits 702 and 704/706 mounted on opposite sides of a single lead frame die paddle 708. *Ma et al* does not teach or suggest mounting one integrated circuit directly on the active surface of another integrated circuit.

Therefore, the rejection of claims 1, 4, 10–11, 13, 16 and 18 under 35 U.S.C. § 102 has been overcome.

35 U.S.C. § 103 (Obviousness)

Claims 2–3, 5–9, 14–15 and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al*. Claims 12 and 19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Ma et al* in view of U.S. Patent No. 5,869,895 to *Raad*. These rejections are respectfully traversed.

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. MPEP § 2142; *In re Fritch*, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. MPEP §

2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Piasecki*, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984). Only when a *prima facie* case of obviousness is established does the burden shift to the applicant to produce evidence of nonobviousness. MPEP § 2142; *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Rijckaert*, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the applicant is entitled to grant of a patent. *In re Oetiker*, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); *In re Grabiak*, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. *In re Bell*, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. MPEP § 2142.

As noted above, independent claims 1 and 13 each recite mounting the second (integrated circuit) chip directly on the active face of the first (integrated circuit) chip, a feature not shown or suggested by the cited portion of *Ma et al.* Similarly, the cited portion of *Raad* fails to teach or suggest mounting an integrated circuit directly on the active face of another integrated circuit. Instead, *Raad* teaches mounting memory device 103 on an electrical contact frame 109, which is in turn mounted "adjacent to the top surface 107" of a microprocessor 101 in contact with electrical contact pads 105 projecting from the surface of microprocessor 101. *Raad*, column 2, line 49 through column 3, line 8. Accordingly, neither reference teaches or suggested mounting an integrated circuit directly on the active face of another integrated circuit.

Therefore, the rejection of claims 2–3, 5–9, 12, 14–15, 17 and 19 under 35 U.S.C. § 103 has been overcome.

AMENDMENTS WITH MARKINGS TO SHOW CHANGES MADE

Claims 2–19 were amended herein as follows:

2. (amended) The microprocessor of claim 1, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

3. (amended) The microprocessor of claim 1, wherein [the central processing unit comprises a field programmable gate array]an active face of the second integrated circuit chip faces the active face of the first integrated circuit chip.

4. (amended) The microprocessor of claim 1, wherein the second integrated circuit chip comprises one of a memory and an analog-to-digital converter.

5. (amended) The microprocessor of claim 4, wherein the [memory]second integrated circuit comprises one of a cache memory, a dynamic random access memory (DRAM), a static random access memory (SRAM), and a flash memory.

6. (amended) The microprocessor of claim [4]1, wherein [the memory comprises DRAM]at least one metal region projecting from the active face of the first integrated circuit chip overlies at least one metal region projecting from a surface of the second integrated circuit chip.

7. (amended) The microprocessor of claim [4]6, wherein the [memory comprises SRAM]second integrated circuit chip is spaced apart from the first integrated chip by a distance of at least a projection height of the at least one metal region projecting from the active face of the first integrated circuit chip plus a projection height of the at least one metal region projecting from the surface of the second integrated circuit chip, wherein the distance is sufficient to permit electrical connection to contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit.

8. (amended) The microprocessor of claim [4]6, [wherein the memory comprises FLASH] further comprising:

a bonding layer between and electrically connecting the at least one metal region projecting from the active face of the first integrated circuit chip and the at least one metal region projecting from a surface of the second integrated circuit chip, wherein the bonding layer provides mechanical bonding of the first and second integrated circuit chips.

9. (amended) The microprocessor of claim 1, [wherein]further comprising:

at least two groups of contact pads on the active surface of the first integrated circuit chip for external connection to the central processing unit, wherein the second integrated circuit chip [comprises an analog-to-digital converter]has a width less than a distance between the two groups of contact pads.

10. (amended) The microprocessor of claim 1, further comprising:

a third integrated circuit chip mounted on, and electrically connected to, the active face of the first integrated circuit adjacent the second integrated circuit chip, wherein the third integrated circuit chip adds further functionality to the central processing unit of the first integrated circuit[microprocessor].

11. (amended) The microprocessor of claim 1, wherein the electrical connection between the first integrated circuit chip and the second integrated circuit chip is by direct connection of [metalizations]metal regions on the active faces of the first and second integrated circuit chips by a bonding layer.

12. (amended) The microprocessor of claim 1, wherein [the first and second integrated circuit chips are further defined as having a profile, and wherein the profile]a length and width of the second integrated circuit chip [is]are less than [the profile]a respective length and width of the first integrated circuit chip.

13. (amended) A microprocessor comprising:

a first chip having an active face including a central processing unit; and

a second chip having an active face, the second chip mounted on, and electrically connected to, the active face of the first chip, wherein the second chip adds functionality to the central processing unit of the first chip and wherein the electrical connection is by a bonding layer between [metalization that is integral with]metal regions on the active faces of the first and second chips.

14. (amended) The microprocessor of claim 13, wherein the [central processing unit comprises a digital signal processor]metal regions further comprise one of:

conductive regions projecting from the active faces of the first and second chips; and

conductive layers over insulating regions projecting from the active faces of the first and second chips,

wherein the active regions of the first and second chips are spaced apart by the metal regions.

15. (amended) The microprocessor of claim 13, wherein the central processing unit comprises one of a digital signal processor and a field programmable gate array.

16. (amended) The microprocessor of claim 13, wherein the second chip comprises one of a memory and an analog-to-digital converter.

17. (amended) The microprocessor of claim 13, wherein [the second chip comprises an analog-to-digital converter]at least one of the metal regions on the active surface of the first chip is disposed over a portion of an integrated circuit forming the central processing unit.

18. (amended) The microprocessor of claim 13, further comprising:

a third chip mounted on, and electrically connected to, the active face of the first chip adjacent the second chip wherein the third chip adds further functionality to the [integrated circuit microprocessor]central processing unit of the first chip.

19. (amended) The microprocessor of claim 13, wherein [the first and second integrated circuit chips are further defined as having a profile, and wherein the profile]a width of the second integrated circuit chip is less than [the profile]a width of the first integrated circuit chip.

SUMMARY

For the reasons given above, the Applicant respectfully requests reconsideration and allowance of pending claims and that this Application be passed to issue. If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this Application, the Applicant respectfully invites the Examiner to contact the undersigned at the telephone number indicated below or at ***dvenglarik@novakov.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

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